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REMARKS

This paper is responsive to the Office Action dated May 13, 2005. Claims 1-4, 6-8, 21-24, 26, 28 and 30 were examined. Claims 1-4, 6-8, 21-24, 26, 28 and 30 remain present in this application, all of which have been rejected. Applicant has made minor amendments to claims 3, 6 and 7 to correct antecedent basis problems.

In the present Office Action, claims 1, 2, 3, 8, 28 and 30 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,881,264 (hereinafter "Kurosawa"); and claims 4, 6, 7, 21-24 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurosawa in view of U.S. Patent 6,473,832 (hereinafter "Ramagopal"). At the outset, Applicant notes that in order for a reference to anticipate a claim, the reference must disclose all limitations of the claim.

Applicant believes that a brief review of one application of Applicant's claimed subject matter may help to move this case toward allowance. With reference to Applicant's Figs. 6 and 7, according to one embodiment of Applicant's claimed subject matter, an instruction is associated with an index 602, e.g. '000', in a scoreboard 600. The index 602, e.g., '000', identifies the instruction, which is associated with a scoreboard entry, e.g., 'rd1', that corresponds to the index 602. Upon receipt of an indication (which includes a corresponding index into the scoreboard) that a terminating event, associated with the instruction, has occurred, the scoreboard entry corresponding to the received index is identified and invalidated. For example, when the indication includes the index '001', the scoreboard entry 'rd2' is invalidated. As is set forth in Applicant's specification, beginning at page 8, line 8, during a decode (D) stage 314, the scoreboard 600 is read and updated. When a new instruction enters the D stage 314, its source and destination register operands are compared with all of the scoreboard entries. If a match is found, the scoreboard 600 is used to provide a hardware interlock between any unfinished load or long-latency operation and a younger instruction that has data/output dependency with the unfinished load or long-latency operation. In such a case, the younger instruction is stalled in the D stage 314 until the unfinished load or long-latency instruction scoreboard entry is terminated, i.e., until a terminating event occurs in relation to the unfinished load or long-latency operation.

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In sum, in the above-described application, the scoreboard is used to stall instructions that try to use results produced by a previous instruction, when the results of the previous instruction are not yet available. When a scoreboard entry is invalidated, a newer instruction, which has data dependency on the previous instruction, is then allowed to utilize the scoreboard.


With specific reference to Kurosawa Fig. 3, Applicant submits that the entry '3758EC' in the Kurosawa scoreboard 130 is a memory address, not an index. Furthermore, Applicant submits that 'No. 2' is not a scoreboard entry (see Fig. 2, reference number 102). To the extent that the entry number 'No. 2' could be considered an index, Applicant submits that Kurosawa does not teach or suggest identifying and invalidating a scoreboard entry based on the entry number, when a terminating event associated with an instruction occurs. The Office Action further asserts that Kurosawa discloses "receiving an indication (synchronization) that a terminal event associated with the instruction has occurred (see the memory access instruction completion in col. 9, lines 1-7), the indication including identifying [see the index of READ instruction 3758ec] and invalidating (see the Invalid bit entry in fig. 3) based on the received scoreboard (see the invalid bit (I) in col. 8, lines 4-12, lines 49-53)." However, Applicant submits that Kurosawa does not teach the utilization of an indication that includes a corresponding index into the scoreboard. Furthermore, Applicant submits that Kurosawa does not teach invalidating a corresponding scoreboard entry based on a received index. For at least these reasons, Applicant submits that independent claims 1 and 28 are allowable over Kurosawa.

With respect to the rejection of independent claim 21 as being unpatentable over Kurosawa in view of Ramagopal, Applicant submits that the discussion with respect to independent claims 1 and 28 is equally applicable to claim 21. Additionally, Applicant submits that neither Kurosawa or Ramagopal, alone or in combination, teach or suggest a load-store unit (see Applicant's Figs. 4 and 7) that returns a scoreboard index that is used to invalidate a scoreboard entry for an instruction. For at least this reason, independent claim 21 is also allowable. Additionally, Applicant submits that the dependent claims 2-4, 6-8, 22-24, 26 and 30 are also allowable for at least the reason that they depend upon allowable claims.

In summary, claims 1-4, 6-8, 21-24, 26, 28 and 30 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is

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respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,



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